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Enclosed herewith for filing is a patent application, as follows:

Inventors Lordson L. Yue, James T. Battle  
Title: Optimal Initial Rasterization Starting Point

- 5 Sheet(s) of Drawings  
14 page(s) Specification  
2 page(s) Claims  
1 page Abstract  
3 page(s) Declaration/Power of Attorney  
1 page(s) Recordation Cover Sheet (in duplicate)  
2 page(s) Assignment  
1 page(s) PTO Form 1449  
☐ Copy(ies) of    Cited References  
☐ Other:

**CLAIMS AS FILED (fees computed under §1.9(f))**

For	Number Filed		Number Extra		Rate		Basic Fee
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Total Claims	6	-20 =	-0-	x	\$18	= \$	-0-
Independent							
Claims	2	-3 =	-0-	x	\$78	= \$	-0-
<input type="checkbox"/> Application contains one or more multiple dependent claims (\$260 total fee)						\$	-0-

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Respectfully submitted,

*Edward C. Kwok*  
Edward C. Kwok  
Attorney for Applicants  
Reg. No. 33,938

## OPTIMAL INITIAL RASTERIZATION STARTING POINT

Lordson L. Yue  
James T. Battle

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BACKGROUND OF THE INVENTION

An image typically includes several objects (e.g.,  
10 a tree, sky or animated character). Each object may be  
computer represented by a group of triangles. Vertex  
data for each triangle includes x and y-coordinate data  
defining the position of each vertex of the triangle  
within the image. In three-dimensional applications,  
15 the vertex data also includes z-coordinate data which  
defines the depth of the triangle in virtual space. On  
a display, a triangle having a greater depth may be  
obscured by a triangle having a lesser depth, thereby  
giving the appearance that the image is three-  
20 dimensional.

In writing each image frame, a graphics processor  
feeds triangle data, one triangle at a time, to a  
rasterizer which assigns luminance and color values to  
25 each pixel location within the triangle. After all  
triangles of the image frame are written into a frame  
buffer, the image frame is displayed. In typical  
graphics applications, an image frame may include many  
thousands of triangles depending on the image  
30 resolution of the image frame. Furthermore, many image  
frames are displayed each second in graphics  
applications. Thus, as the graphics applications  
become more complex, the graphics processor and  
rasterizer must operate faster.

35

SUMMARY OF THE INVENTION

Images may be represented as a group of triangles. A rasterizer assigns pixel values corresponding to one triangle at a time to a frame buffer, each triangle represented by vertex data. In one embodiment, a frame buffer is divided into tiles of, for example, 32 by 32 pixels. Triangles (and portions thereof) that are within a current tile are rasterized one triangle at a time into the tile location. This process repeats for each tile in the image frame. For graphics applications, this process repeats for each image frame in the graphics stream.

15 In accordance with the present invention, vertex data corresponding to three vertices of a triangle are received in a sorting circuit. The sorting circuit generates control bits representing an order of the vertices along, for example, the vertical direction. A multiplexer passes data corresponding to one (e.g., the highest) of the vertices in response to the control bits. Similarly, other multiplexers may pass data corresponding to the middle and lowest vertices. Thus, the vertices of the triangle are sorted through the multiplexers such that the ordering of the vertices after the multiplexer is predictable. This predictability simplifies the downstream logic circuit by reducing the vertex position permutations that the downstream logic circuit may encounter.

30 A region calculation circuit generates region bits representing a location of each of the vertices with respect to a current tile. A trivial discard of the triangle data occurs if the region bits indicate that the entire triangle lies outside of the tile. For example, a trivial discard occurs if the region bits

indicate that the lowest vertex is higher than the top edge of the tile, that the highest vertex is lower than the bottom edge of the tile, that all the vertices are left of the left edge of the tile, or that all the  
5 vertices are right of the right edge of the tile.

After the trivial discard, initial rasterization starting point estimate coordinates are generated for the rasterizer. This starting point estimate lowers  
10 the time needed for the rasterizer to find the first pixel of the current triangle to be assigned values. The starting point may be generated using the region bits.

15 The principles of the present invention will best be understood in light of the following detailed description along with the accompanying drawings.

20 BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic diagram of a setup engine according to the invention.

25 Fig. 2 is a detailed diagram of the initial rasterization starting point estimation circuit of Fig. 1.

30 Figs. 3A, 3B, 3C, 3D, 3E and 3F show various permutations of y-coordinate ordering of triangle vertices.

Fig. 4 shows the current tile and eight surrounding regions.  
35

Fig. 5 shows four triangles that are trivially discarded and one which is not.

Fig. 6 shows a triangle that is trivially  
5 accepted.

Fig. 7 shows a triangle of which the highest vertex lies north of the current tile.

10 Fig. 8 shows a triangle of which line 0'1' is the highest line of the triangle to intersect LEFT\_EDGE.

Fig. 9 shows a triangle of which line 1'2' is the highest line of the triangle to intersect LEFT\_EDGE.  
15

Fig. 10 shows a triangle of which line 0'2' is the highest line of the triangle to intersect LEFT\_EDGE.

Fig. 11 shows a triangle of which line 0'1' is the highest line of the triangle to intersect RIGHT\_EDGE.  
20

Fig. 12 shows a triangle of which line 1'2' is the highest line of the triangle to intersect RIGHT\_EDGE.

25 Fig. 13 shows a triangle of which line 0'2' is the highest line of the triangle to intersect RIGHT\_EDGE.

#### DETAILED DESCRIPTION OF THE INVENTION

30

In this description, the same or similar elements in different drawings are identified with the same reference symbols. In this description, "&" means logical AND, "+" means logical OR, and "!" means  
35 logical NOT. Items within parentheses "()" have

highest logical priority followed by "!", "&", and "+", in descending priority order.

A frame buffer (not shown) may be divided into  
 5 tiles of, for example, 32 by 32 pixels. Triangles (and portions thereof) that are within a given tile are rasterized one triangle at a time into the tile location. This process repeats for each tile in the image frame. For graphics applications, this process  
 10 repeats for each image frame in the graphics stream.

Fig. 1 shows a setup engine 101 that receives triangle vertex data v0, v1 and v2 from a vertex data feeding circuit 100, and provides data including an  
 15 initial rasterization starting point estimate ("IRSPE") to a rasterizer 102. Although the vertex data v0, v1 and v2 are shown transmitted over three separate buses in Fig. 1, the vertex data v0, v1 and v2 may also be transmitted serially over a single bus as is known in  
 20 the art. Vertex data v0, v1 and v2 represent a corresponding vertex 0, 1 and 2 of a triangle 103 to be set up for rasterization. The vertex data v0, v1 and v2 include, but are not limited to, x-coordinate components v0.x, v1.x and v2.x and y-coordinate  
 25 components v0.y, v1.y and v2.y, respectively. The vertex data v0, v1 and v2 may also include, z-coordinate, color, blending and texture data, and other data as desired.

30 Setup engine 101 transforms the vertex data v0, v1 and v2 by 1) sorting the vertex data v0, v1 and v2 in y-coordinate order, 2) trivially discarding vertex data of triangles entirely outside of the current tile, 3) estimating an initial rasterization starting point that  
 35 minimizes the searching by rasterizer 102 required to find the rasterization starting point of the triangle

103, and 4) any other operations on v0, v1 and v2 as desired. Rasterizer 102 draws whatever portions of triangle 103 that are within a given tile into a frame buffer (not shown).

5

Setup engine 101 sorts vertex data v0, v1 and v2 in y-coordinate order to simplify the downstream logic circuit as the number of permutations the downstream logic circuit must deal with is reduced due to the predictability of the y-ordering. Of course, this ordering may be in descending or ascending y-coordinate order as long as the y-positioning of the vertex is made predictable. Furthermore, if the rasterizer rasterizes vertically, setup engine 101 may sort the vertices according to the x-coordinate. For clarity, in the example that follows, the vertices are described as being sorted in descending y-coordinate order.

A y-sort circuit 110 receives the y-coordinate data v0.y, v1.y and v2.y, and generates control bits y01, y02, and y12 which cause multiplexers 150, 151 and 152 to sort the vertex data v0, v1 and v2 in, for example, descending y-coordinate order. Bit y01 has a value 1 only if v0.y is greater than v1.y, bit y02 has a value 1 only if v0.y is greater than v2.y, and bit y12 has a value 1 only if v1.y is greater than v2.y. Table 1 summarizes the y-coordinate ordering given input bits y01, y02 and y12.

case #	y01	y02	y12	v0.y	v1.y	v2.y	Fig.
0	1	1	1	highest	middle	lowest	3A
1	1	1	0	highest	lowest	middle	3B
2	1	0	1	-	-	-	none
3	1	0	0	middle	lowest	highest	3C
4	0	1	1	middle	highest	lowest	3D
5	0	1	0	-	-	-	none
6	0	0	1	lowest	highest	middle	3E
7	0	0	0	lowest	middle	highest	3F

Table (1)

- 5 The six possible cases 0, 1, 3, 4, 6 and 7 of Table (1) for the y-coordinate ordering of the three vertices are shown respectively in Figs. 3A, 3B, 3C, 3D, 3E and 3F.

- 10 In response to control bits y01, y02 and y12, multiplexer 150 passes the vertex data having the highest y-coordinate value (v0 in cases 0 and 1, v1 in cases 4 and 6, and v2 in cases 3 and 7) into memory 160. Multiplexer 151 passes the vertex data having the middle y-coordinate value (v0 in cases 3 and 4, v1 in cases 0 and 7, and v2 in cases 1 and 6) into memory 161. Multiplexer 152 passes the vertex data having the lowest y-coordinate value (v0 in cases 6 and 7, v1 in cases 1 and 3, and v2 in cases 0 and 4) into memory 162. Hereinafter, the vertex data in memories 160, 161 and 162 are respectively referred to as "highest vertex data V0", "middle vertex data V1" and "lowest vertex data V2" corresponding to the sorted vertices 0', 1' and 2' of triangle 103'. Y-sorting of the vertex data is thus completed.

25



After sorting, a trivial discard analysis occurs as follows. Fig. 4 shows the current tile TILE and eight surrounding regions 401-408. TILE is defined by edges TOP\_EDGE, RIGHT\_EDGE, BOTTOM\_EDGE and LEFT\_EDGE.

5 Hereinafter, the x-coordinate position of LEFT\_EDGE and RIGHT\_EDGE is LEFT\_EDGE.x and RIGHT\_EDGE.x, respectively. The y-coordinate position of TOP\_EDGE and BOTTOM\_EDGE is TOP\_EDGE.y and BOTTOM\_EDGE.y, respectively.

10

Referring to Fig. 1, a region calculation circuit 120 reads the permuted x-coordinate data (V0.x, V1.x and V2.x), the sorted y-coordinate data (V0.y, V1.y and V2.y), and the tile boundaries TOP\_EDGE.y,

15

BOTTOM\_EDGE.y, LEFT\_EDGE.x and RIGHT\_EDGE.x. Based on these values, region calculation circuit 120 generates region bits n0, n1, n2, e0, e1, e2, s0, s1, s2, w0, w1 and w2 representing the position of the sorted vertices 0', 1' and 2' with respect to TILE.

20

Referring to Fig. 4, vertex  $i'$  (where  $i$  is 0, 1 or 2) is considered north ( $n_i = 1$ ) of TILE if its y-coordinate is greater than TOP\_EDGE.y (regions 408, 401 and 402 of Fig. 4), east ( $e_i = 1$ ) of TILE if its x-coordinate is greater than RIGHT\_EDGE.x (regions 402, 403 and 404), south ( $s_i = 1$ ) of TILE if its y-coordinate is less than BOTTOM\_EDGE.y (regions 406, 405 and 404 of Fig. 4), and west ( $w_i = 1$ ) of the tile if its x-coordinate is less than LEFT\_EDGE.x (regions 408, 407 and 406 of Fig. 4).

30

An orientation circuit 130 generates a bit CW having a value 1 only if the line ("line 0'2'") connecting vertex 0' and 2' is oriented clockwise from the line ("line 0'1'") connecting vertex 0' and 1'. In

35

other words, orientation circuit 130 assigns a value 1 to bit CW only if Equation (1) is true.

$$(V0.x-V1.x)(V0.y-V2.y) < (V0.x-V2.x)(V0.y-V1.y) \quad (1)$$

5

Y-sort circuit 110, region calculation circuit 120 and orientation circuit 130 all have access to a comparator 140 to perform the above comparisons.

10 The region bits n0, n1, n2, e0, e1, e2, s0, s1, s2, w0, w1 and w2; the orientation bit CW; and the vertex data V0, V1 and V2 are inputted into IRSPE circuit 170 (Fig. 1) shown in further detail in Fig. 2. IRSPE circuit 170 may be, for example, a portion of a

15 larger setup operational unit.

Referring to Fig. 2, IRSPE circuit 170 trivially discards the triangle 103 under certain conditions as shown in Table (2) in which the triangle lies

20 completely outside of TILE.

Case #	trivial discard if true	rationale for trivial discard
1	n2 = 1	implies entire triangle is north of TILE (i.e., north of TOP_EDGE)
2	s0 = 1	implies entire triangle is south of TILE (south of BOTTOM_EDGE)
3	w0&w1&w2 = 1	implies entire triangle is west of TILE (i.e., west of LEFT_EDGE)
4	e0&e1&e2 = 1	implies entire triangle is east of TILE (i.e., east of RIGHT_EDGE)

Table (2)

25 Cases 1, 2, 3 and 4 are shown respectively as triangles 501, 502, 503 and 504 of Fig. 5. If any one of cases 1

to 4 of Table (2) is true, trivial discard circuit 208 generates a bit y308 of a value 1, causing setup engine 101 (Fig. 1) to request the next triangle for TILE without providing data to rasterizer 102 (Fig. 1).

5

Note that bit y308 sometimes has a value 0 even though the triangle (e.g., triangle 505 of Fig. 5) lies entirely outside of TILE. Performing a discard step for all triangles that are entirely outside of TILE would be computationally intensive and might slow down the triangle setup procedure.

10

If none of the trivial discard cases are true (i.e., bit y308 has a value 0), setup engine 101 estimates an initial rasterization starting point. This reduces the number of cycles required for rasterizer 102 to find the first pixel that requires assignment of luminance and/or color values.

15

20

A typical rasterizer checks each pixel in a field (e.g., a tile or frame) to determine if the pixel is positioned within an object (e.g., a triangle). If not, the rasterizer proceeds to the next pixel and so on in a raster pattern until a pixel is found which is positioned in the object. Once a pixel within the object is found, there are numerous conventional ways to reduce the number of pixels checked by a rasterizer before the object is entirely rasterized. However, often significant time is taken finding a pixel that lies within the object. Setup engine 101 (Fig. 1) provides rasterizer 102 (Fig. 1) with initial rasterization starting point estimation coordinates IRSPE.x and IRSPE.y to reduce this time.

25

30

35

Specifically, referring to Fig. 2, IRSPE circuit 170 generates control bits y312, y316, y320, y324,

y328, y332, y336 and y340 causing multiplexers 260 and 270 to pass the estimate coordinates IRSPE.x and IRSPE.y as described below.

- 5 Trivial accept circuit 212 assigns a value 1 to bit y312 only if !n0&!e0&!s0&!w0 equals 1, in which case the highest vertex 0' lies within the selected tile as in triangle 601 of Fig. 6. If bit y312 has value 1, multiplexers 260 and 270 pass the actual  
10 coordinates V0.x and V0.y of the top vertex 0 as IRSPE.x and IRSPE.y.

- Circuit 216 assigns a value 1 to bit y316 only if n0&!e0&!w0 equals 1, in which case the highest vertex  
15 0' lies directly north of TILE as in triangle 701 of Fig. 7. Since there has been no trivial discard of triangle 103', triangle 103' does not lie entirely north of TOP\_EDGE. Thus, the line 0'2' must intersect with TOP\_EDGE if bit y316 has a value 1. A bit y316 of  
20 value 1 causes an intercept calculation circuit 280 to output value INT representing the x-intercept of line 0'2' with TOP\_EDGE, the value INT being horizontally clamped right to LEFT\_EDGE.x or left to RIGHT\_EDGE.x if needed. A bit y316 of value 1 causes multiplexers 260  
25 and 270 to pass INT as IRSPE.x and TOP\_EDGE.y as IRSPE.y.

- Circuit 220 assigns a value 1 to bit y320 only if w0&!w1&CW has a value 1, in which case the line 0'1' is  
30 the highest line of the triangle to intersect LEFT\_EDGE as in triangle 801 of Fig. 8. A bit 320 of value 1 causes the intercept calculation circuit 280 to assign, as value INT, the y-intercept of line 0'1' with LEFT\_EDGE, the value INT being vertically clamped down  
35 to TOP\_EDGE if INT is higher than TOP\_EDGE, or clamped up to BOTTOM\_EDGE if INT is lower than BOTTOM\_EDGE.

Hereinafter, this clamping is referred to as "vertical clamping". A bit y320 of value 1 causes multiplexers 260 and 270 to pass LEFT\_EDGE.x as IRSPE.x and INT as IRSPE.y.

5

Circuit 224 assigns a value 1 to bit y324 only if  $w0 \& w1 \& CW$  equals 1. Since no trivial discard has occurred, the triangle does not lie entirely west of LEFT\_EDGE. Thus, w2 must have a value 0. In this case, line 1'2' is the highest line of the triangle to intersect LEFT\_EDGE as in triangle 901 of Fig. 9. A bit 324 of value 1 causes the intercept calculation circuit 280 to assign, as value INT, the vertically clamped y-intercept of line 1'2' with LEFT\_EDGE. A bit y324 of value 1 causes multiplexers 260 and 270 to pass LEFT\_EDGE.x as IRSPE.x and INT as IRSPE.y.

Circuit 228 assigns a value 1 to bit y328 only if  $w0 \& !CW$  equals 1. Since no trivial discard has occurred, line 0'2' is the highest line to intersect LEFT\_EDGE as in triangle 1001 of Fig. 10. A bit 328 of value 1 causes the intercept calculation circuit 280 to assign, as value INT, the vertically clamped y-intercept of line 0'2' with LEFT\_EDGE. A bit y328 of value 1 causes multiplexers 260 and 270 pass LEFT\_EDGE.x as IRSPE.x and INT as IRSPE.y.

Circuit 232 assigns a value 1 to bit y332 only if  $e0 \& !e1 \& !CW$  equals 1, in which case the line 0'1' is the highest line to intersect RIGHT\_EDGE as in triangle 1101 of Fig. 11. A bit 332 of value 1 causes the intercept calculation circuit 280 to assign, as value INT, the vertically clamped y-intercept of line 0'1' with RIGHT\_EDGE. A bit y332 of value 1 causes multiplexers 260 and 270 pass RIGHT\_EDGE.x as IRSPE.x and INT as IRSPE.y.

Circuit 336 assigns a value 1 to bit y336 only if e0&e1&!CW equals 1, in which case the line 1'2' is the highest line to intersect RIGHT\_EDGE as in triangle 1201 of Fig. 12. A bit 336 of value 1 causes the intercept calculation circuit 280 to assign, as value INT, the vertically clamped y-intercept of line 1'2' with RIGHT\_EDGE. A bit y336 of value 1 causes multiplexers 260 and 270 to pass RIGHT\_EDGE.x as IRSPE.x and INT as IRSPE.y.

Circuit 240 assigns a value 1 to bit y340 only if e0&CW equals 1, in which case, since no trivial discard has occurred, the line 0'2' is the highest line to intersect RIGHT\_EDGE as in triangle 1301 of Fig. 13. A bit 340 of value 1 causes the intercept calculation circuit 280 to assign, as value INT, the vertically clamped y-intercept of line 0'2' with RIGHT\_EDGE. A bit y340 of value 1 causes multiplexers 260 and 270 to pass RIGHT\_EDGE.x as IRSPE.x and INT as IRSPE.y.

Thus, an initial rasterization starting point is estimated. Rasterizer 102 may now find the rasterization starting point faster using coordinates IRSPE.x and IRSPE.y. Note that assuming no trivial discard has occurred, exactly one of bits 312, 316, 320, 324, 328, 332, 336 and 340 has a value 1.

This process is repeated for all triangles within the selected tile, and for all tiles within the image frame. Although the above describes a specific embodiment of the present invention, this embodiment is illustrative only and not limiting. Various modifications and substitutions will be apparent to one skilled in the art. All such modifications and substitutions are intended to be part of the present

invention. The invention is defined by the following claims.

CLAIMS

We claim:

- 5           1.    A method comprising:  
              receiving, in a circuit, first, second and  
              third vertex data corresponding to first, second  
              and third vertices of a triangle;  
              generating, in the circuit, region bits  
10           representing a location each of the first, second,  
              and third vertices with respect to a tile being  
              rendered; and  
              outputting coordinate data to a rasterizer,  
              the coordinate data representing an initial  
15           rasterization starting point estimate based on the  
              region bits.
2.    The method of Claim 1, further comprising:  
              generating, in the circuit, an orientation  
20           bit representing an orientation of a line  
              connecting the first and second vertices with a  
              line connecting the first and third vertices.
3.    The method of Claim 2, further comprising:  
25           sorting the first, second and third vertices  
              according to a position in a predetermined  
              direction.
4.    A circuit comprising:  
30           a region calculation circuit configured to  
              receive vertex data corresponding to vertices of a  
              triangle, the region calculation circuit  
              configured to generate region bits representing a  
              position of the vertices with respect to a tile  
35           being rendered; and



an initial rasterization starting point estimation circuit configured to receive the region bits and generate an initial rasterization starting point estimate coordinates.

5

5. The circuit of Claim 4, further comprising:  
an orientation circuit configured to generate an orientation bit representing an orientation of a line connecting a first vertex and a second vertex of the triangle with respect to a line connecting the first vertex and a third vertex of the triangle.

10

6. The circuit of Claim 4, further comprising:  
a rasterizer configured to receive the initial rasterization starting point estimation circuit coordinates.

15

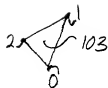
## OPTIMAL INITIAL RASTERIZATION STARTING POINT

Lordson L. Yue  
James T. Battle

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ABSTRACT OF THE DISCLOSURE

A frame buffer is divided into tiles of, for  
10 example, 32 by 32 pixels. Triangles (and portions thereof) that are within a given tile are rasterized one triangle at a time into the tile location. This process repeats for each tile in the image frame. A sorting circuit generates control bits representing a  
15 vertical order of the vertices of a current triangle. A series of multiplexers vertically sorts the vertices bases on these control bits. A region calculation circuit generates region bits representing a location each of the vertices with respect to the current tile.  
20 A trivial discard of the triangle data occurs if the region bits indicate that the entire triangle lies outside of the tile. Subsequently, an initial rasterization starting point is estimated based on the region bits to lower the time needed for the rasterizer  
25 to find the first pixel of the current triangle to be assigned values.

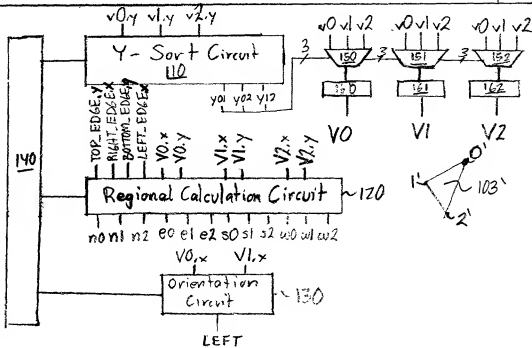


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# Vertex Data Feeding Circuit 100

v0 v1 v2

101



n0 n1 n2 e0 e1 e2 s0 s1 s2 w0 w1 w2 LEFT v0 v1 v2

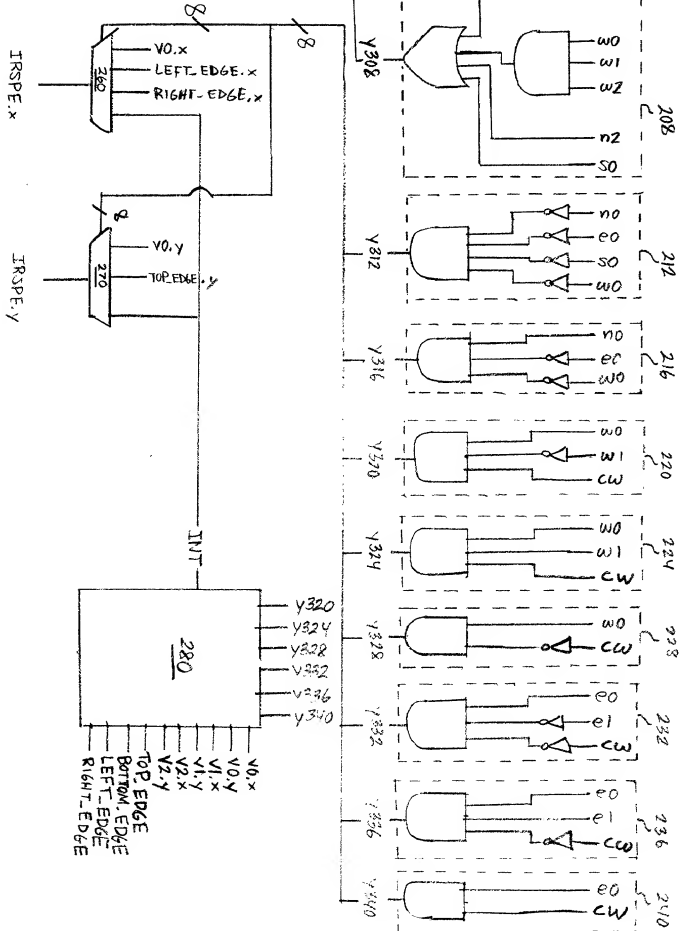
Initial  
Rasterization  
Starting  
Point  
Estimation  
Circuit  
170

IRSPE

Rasterizer 102

F16.1

170



FILE 2

3/5

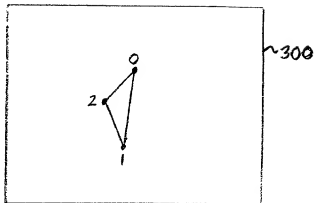


FIG. 3B

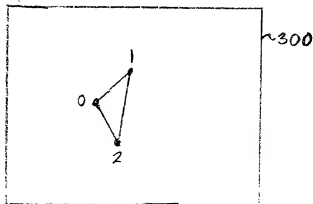


FIG. 3D

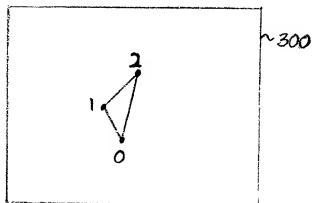


FIG. 3F

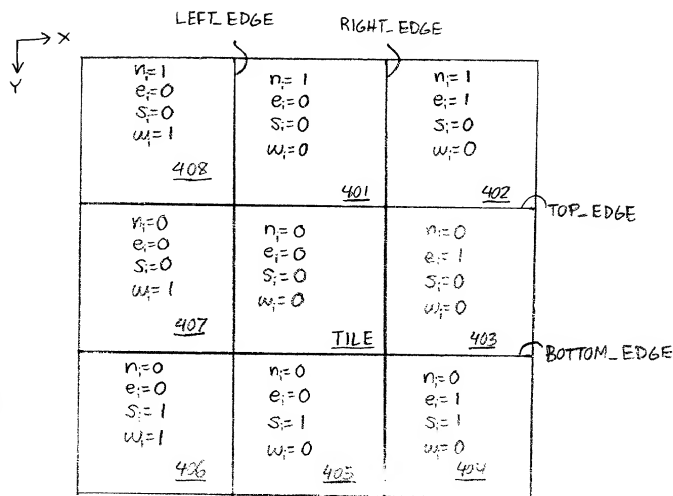


FIG. 4

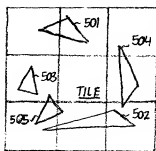


FIG. 5

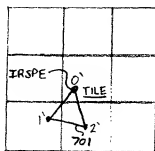


FIG. 6

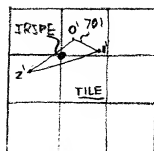


FIG. 7

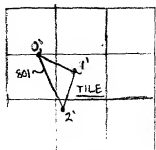


FIG. 8

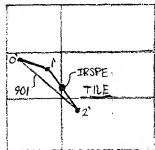


FIG. 9

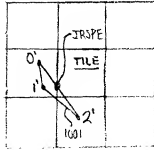


FIG. 10

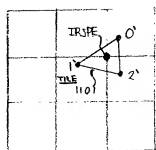


FIG. 11

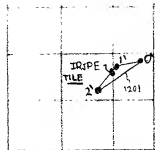


FIG. 12

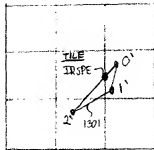


FIG. 13

## DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below adjacent to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of subject matter (process, machine, manufacture, or composition of matter, or an improvement thereof) which is claimed and for which a patent is sought by way of the application entitled

### Optimal Initial Rasterization Starting Point

which (check) ☒ is attached hereto.

☐ and is amended by the Preliminary Amendment attached hereto.

☐ was filed on \_\_\_\_\_ as Application Serial No. \_\_\_\_\_

☐ and was amended on \_\_\_\_ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information, which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) of any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
Number	Country	Day/Month/Year Filed	Yes	No
N/A			<input type="checkbox"/>	<input type="checkbox"/>

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

Provisional Application Number	Filing Date
N/A	

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or PCT international application(s) designating the United States of America listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the



duty to disclose information, which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56, which became available between the filing date of the prior application(s) and the national or PCT international filing date of this application:

Application Serial No.	Filing Date	Status (patented, pending, abandoned)
N/A		

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith:

Alan H. MacPherson (24,423); Thomas S. MacDonald (17,774); Brian D. Ogonowsky (31,988); David W. Heid (25,875); Norman R. Klivans (33,003); Edward C. Kwok (33,938); David E. Steuber (25,557); Michael Shenker (34,250); Stephen A. Terrile (32,946); Peter H. Kang (40,350); Ronald J. Meetin (29,089); Ken John Koestner (33,004); Omkar K. Suryadevara (36,320); David T. Millers (37,396); Kent B. Chambers (38,839); Serge J. Hodgson (40,017); Michael P. Adams (34,763); Michael J. Halbert (40,633); Gary J. Edwards (41,008); William B. Tiffany (41,347); James E. Parsons (34,691); Daniel P. Stewart (41,332); Philip W. Woo (39,880); John T. Winburn (26,822); Tom Chen (42,406); Fabio E. Marino (43,339); William W. Holloway (26,182); Elaine H. Lo (41,158); Don C. Lawrence (31,975); Marc R. Ascolese (42,268); Carmen C. Cook (42,433); David G. Dolezal (41,711); Adrian J. Lee (42,785); Michael P. Noonan (42,038); Roberta P. Saxon (43,087); Bernice Chen (42,403); Mary Jo Bertani (42,321); Dale R. Cook (42,434); Matthew J. Brigham (44,047); Robert B. Morrill (43,817); Glen B. Choi (43,546); Hugh H. Matsubayashi (43,779); Margaret M. Kelton (44,182); Joseph T. VanLeeuwen (44,383); Sam G. Campbell (42,381); Mark Grant (36,151); Eugene Conser (39,149); Coleman Reif (38,593); Allen Tremain (40,207); and Ronald L. Taylor (27,161).

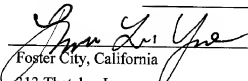
Please address all correspondence and telephone calls to:

Edward C. Kwok  
 Attorney for Applicant(s)  
**SKJERVEN, MORRILL, MacPHERSON, FRANKLIN & FRIEL LLP**  
 25 Metro Drive, Suite 700  
 San Jose, California 95110-1349

Telephone: 408-453-9200  
 Facsimile: 408-453-7979

I declare that all statements made herein of my own knowledge are true, all statements made herein on information and belief are believed to be true, and all statements made herein are made with the knowledge that whoever, in any matter within the jurisdiction of the Patent and Trademark Office, knowingly and willfully falsifies, conceals, or covers up by any trick, scheme, or device a material fact, or makes any false, fictitious or fraudulent statements or representations, or makes or uses any false writing or document knowing the same to contain any false, fictitious or fraudulent statement or entry, shall be subject to the penalties including fine or imprisonment or both as set forth under 18 U.S.C. 1001, and that violations of this paragraph may jeopardize the validity of the application or this document, or the validity or enforceability of any patent, trademark registration, or certificate resulting therefrom.

Full name of first joint inventor: Lordson L. Yue

Inventor's Signature: 

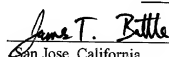
Date: 1/27/99

Residence: Foster City, California

Post Office Address: 313 Thatcher Lane  
Foster City, California 94404

Citizenship: USA

Full name of second joint inventor: James T. Battle

Inventor's Signature: 

Date: 1/27/99

Residence: San Jose, California

Post Office Address: 110 South Fifteenth Street  
San Jose, California 95112

Citizenship: USA